

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	1	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and (central near3 tap) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 13:34
L5	1	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and (center near3 tap) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 13:34
L7	1	((drawn or spiral) near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification)) and (center near3 tap)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 13:47
L8	9	(spiral adj inductor) same (center near3 tap)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:49
L9	1	inductor with spiral with tap with (center or centre) with binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:50
L10	1	inductor with spiral with tap with (center or centre) and binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:51
L11	2	inductor with spiral same binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:54
L12	2	inductor same spiral same binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:54

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L13	189	inductor same spiral and binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 14:54
L14	4	inductor same spiral same tap and binary	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 15:06
L15	56	inductor same (binary near3 data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 15:08
L16	1	inductor same (binary near3 data) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 15:07
L17	2	inductor same (binary near3 data) same layer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 15:08
S2	1	(drawn near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic)) and spir\$3 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:43
S3	3	(drawn near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic)) and spir\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:47
S4	1	(drawn near3 induct\$3) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:45
S5	1036	(drawn near3 induct\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:45
S6	3	inductor same LVS and spir\$3 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:46

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S7	79	((drawn or spiral) near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification)) and spir\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 12:48
S9	2	((drawn or spiral) near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification)) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:09
S10	1	(drawn near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic)) and spir\$3 and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:55
S11	2	"20050229126"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:52
S12	87	((drawn or spiral) near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 13:43
S13	24	((drawn or spiral) near3 induct\$3) and (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:12
S14	11	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 08:01
S15	10	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 08:26

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S17	6	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and uniform and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 08:29
S18	1	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and (uniform near3 width) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 08:29
S19	2	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer and (uniform near3 width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 13:33
S20	1588	((drawn or spiral) near3 induct\$3) same (LVS or (layout adj versus adj schematic) or (layout adj vs adj2 schematic) or (physical near3 verification) or verif\$3 or verificat\$3 or test\$3 or analyz\$3 or analysis) and layer uniform and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 12:43


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 Lee, J.; Lee, S.; Roblin, P.; Bibyk, S.;  
[SoutheastCon, 2005. Proceedings. IEEE](#)  
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 Digital Object Identifier 10.1109/SECON.2005.1423229  
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- ☐ 2. **Robust automated synthesis methodology for integrated sp variability**  
 Nieuwoudt, A.; Massoud, Y.;  
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- ☐ 3. **High performance spiral inductors embedded on organic su applications**  
 Lee, S.H.; Min, S.; Kim, D.; Dalmia, S.; Kim, W.; Sundaram, V.; E  
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- ☐ 4. **Analysis, design, and optimization of spiral inductors and tr RF ICs**  
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- ☐ **5. A simple systematic spiral inductor design with perfected Q CMOS RFIC application**  
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- ☐ **6. Design and analysis of novel compact inductor resonator filter**  
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- ☐ **7. A broadband and scalable model for on-chip inductors in CMOS and conductor loss effects**  
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- ☐ **8. The modeling, characterization, and design of monolithic integrated RF IC's**  
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- ☐ **10. A simple systematic procedure of Si-based spiral inductor circuit**  
Chih-Yuan Lee; Tung-Sheng Chen; Chin-Hsing Kao; Deng, J.D.  
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- ☐ **11. A broadband and scalable model for on-chip inductors in CMOS and conductor loss effects**  
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- ☐ **12. Analysis and optimization of monolithic inductors and trans**  
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- ☐ **13. Computer aided design of square spiral transformers and its**  
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- ☐ **14. Winding geometrical effects on the high frequency loss of inductor**  
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- ☐ **15. Frequency-dependent analytical modeling of integrated inductor**  
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- ☐ **16. Application of micro-genetic algorithm (MGA) to a class of circuit**  
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- ☐ **17. Optimization of high Q CMOS-compatible microwave inductor**  
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- ☐ **18. Study of geometrical effects on the high frequency winding inductor design**  
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- ☐ **19. Optimizing the design of spiral inductors on silicon**  
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- ☐ **20. Optimization of high Q CMOS-compatible microwave induct CMOS technology**  
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- ☐ **21. Analysis of multi-layer integrated inductors with wave conc procedure (WCIP)**  
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- 22. Wideband Passive Multi-Port Model Order Reduction and R Circuits**  
Qi Zhenyu ; Yu Hao ; Liu Pu ; Tan Sheldon ; He Lei ;  
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**IEEE STD** IEEE Standard

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- ☐ **1. Physical modeling of spiral inductors on silicon**  
Yue, C.P.; Wong, S.S.;  
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- ☐ **2. Centre-tapped spiral inductors for monolithic band**  
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- ☐ **4. Computer aided design of square spiral transform inductors [MIC application]**  
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